Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (currently amended) An electronic component ~~chip structure,~~ comprising:

a semiconductor substrate; ~~having a plurality of electronic devices positioned on or in a surface layer of said semiconductor substrate;~~

a metallization structure over said semiconductor substrate; ~~fine line interconnection scheme comprising:~~

~~a plurality of dielectric layers over said semiconductor substrate, said dielectric layers having a plurality of via holes; and~~

~~a plurality of circuit layers each on one of said dielectric layers, wherein said circuit layers are electrically connected to each other through said via holes and are electrically connected to said electronic device~~

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and~~fine line interconnection scheme, wherein said passivation layer comprises at least a opening exposing portion of the most top circuit layer;~~

a patterned circuit layer connected to said top surface, wherein said patterned circuit layer comprises a first portion having a bump formed thereover and a second portion used to be tested thereto. ~~a post-passivation scheme over said passivation layer and electrically connected to said circuit layers, wherein said post-passivation scheme comprises at least a bump pad and at least a testing pad, said testing pad electrically connecting to said bump pad; and~~

~~at least a bump over said bump pad.~~

2. (currently amended) The electronic component ~~chip structure~~ of Claim 1, wherein said patterned circuit layer comprises gold. ~~post passivation scheme comprising at least one metal layer, wherein said metal layer is a composite structure comprising an adhesion/barrier layer at the bottom and a gold layer at the top, said gold layer having a thickness greater than 1 μm.~~

3. (currently amended) The electronic component ~~chip structure~~ of Claim 1~~-2~~, wherein said patterned circuit layer comprises a gold layer having a thickness greater than 1 micron. ~~said adhesion/barrier layer consisting of material selected from a group of chromium, titanium, tantalum, titanium-tungsten alloy, tantalum nitride and titanium nitride.~~

4. (currently amended) The electronic component ~~chip structure~~ of Claim 1, wherein said patterned circuit layer comprises copper. ~~post passivation scheme comprising at least one metal layer, and wherein said metal layer is a composite structure comprising an~~

~~adhesion/barrier layer and a copper layer; said copper layer formed on top of said adhesion/barrier layer.~~

5. (currently amended) The electronic component ~~chip structure~~ of Claim 1~~-4~~, wherein said patterned circuit layer comprises nickel. ~~the material constituting said adhesion/barrier layer is selected from a group consisting of chromium, titanium, tantalum, titanium tungsten alloy, titanium nitride and tantalum nitride.~~

6. (currently amended) The electronic component ~~chip structure~~ of Claim 1~~-4~~, wherein said patterned circuit layer comprises a copper layer and a gold layer, said gold layer being over said copper layer. ~~metal layer further comprises a nickel layer formed on top of said copper layer.~~

7. (currently amended) The electronic component ~~chip structure~~ of Claim 6, wherein said patterned circuit layer further comprises a nickel layer between said copper layer and said gold layer. ~~metal layer further comprises a gold layer formed on top of said nickel layer.~~

8. (currently amended) The electronic component ~~chip structure~~ of Claim 1 further comprising a polymer layer over said passivation layer, wherein said patterned circuit layer is over said polymer layer. ~~post passivation scheme comprises at least a metal layer and a polymer layer disposed between said metal layer and said passivation layer.~~

9. (currently amended) The electronic component ~~chip structure~~ of Claim 8, wherein said polymer layer comprises ~~is~~ polyimide. ~~, benzocyclobutene, porous dielectric material, parylene, epoxy, solder mask material or elastomer.~~

10. (currently amended) The chip structure of Claim 1 further comprising a polymer layer on said patterned circuit layer, an opening in said polymer layer exposing said first portion. ~~, wherein said post-passivation scheme comprises at least a metal layer and a polymer layer covering said metal layer, said polymer layer having a plurality of openings exposing said testing pad or said bump pad.~~

11. (currently amended) The electronic component ~~chip structure~~ of Claim 10, wherein said polymer layer comprises ~~is~~ polyimide. ~~, benzocyclobutene, porous dielectric material, parylene, epoxy, solder mask material or elastomer.~~

Claim 12 (canceled)

13. (currently amended) The electronic component ~~chip structure~~ of Claim 1, wherein said patterned circuit layer comprising a metal trace connecting said first and second portions. ~~post-passivation scheme comprising a top metal layer, wherein said top metal layer comprises at least a metal line connecting the bump pad to the testing pad.~~

Claim 14 (canceled)

15. (currently amended) The electronic component ~~chip structure~~ of Claim 1, wherein said passivation layer comprises a topmost nitride layer of said electronic component. ~~opening of the passivation layer has a width larger than about 0.1 μm.~~

16. (currently amended) The electronic component ~~chip structure~~ of Claim 1, wherein said passivation layer has a thickness greater ~~larger~~ than 0.35 μm.

17. (currently amended) The electronic component ~~chip structure~~ of Claim 1 further comprising a bump on said first portion. ~~, wherein said passivation layer is a silicon oxide layer, a silicon nitride layer, a phosphosilicate glass (PSG) layer, a silicon oxide nitride layer or a composite structure comprising the above mentioned layers.~~

18. (currently amended) The electronic component ~~chip structure~~ of Claim 17 further comprising a nickel layer between said bump and said first portion. ~~1, wherein said post passivation scheme comprises at least a top metal layer, wherein said top metal layer having a thickness larger than 0.4 μm.~~

19. (currently amended) The electronic component ~~chip structure~~ of Claim 17 ~~1~~, wherein said bump comprises solder. ~~a solder metal and an under bump metallurgy layer, said under bump metallurgy layer is disposed on said bump pad and said solder metal is disposed on said under bump metallurgy layer.~~

20. (currently amended) The electronic component ~~chip structure~~ of Claim 17~~-19~~, further comprising a copper layer between said bump and said first portion. ~~wherein said under-bump-metallurgy layer is formed, from the bottom to the top, from a titanium layer, a copper layer, and a nickel layer.~~

21. (currently amended) The electronic component ~~chip structure~~ of Claim 17~~-19~~, wherein said bump comprises a lead-free alloy. ~~a material constituting the solder metal is selected from a group consisting of a tin-lead solder alloy and a lead-free solder alloy.~~

Claim 22 (canceled)

23. (currently amended) The electronic component ~~chip structure~~ of Claim 1, wherein said patterned circuit layer comprises a third portion used to be wirebonded thereto. ~~post-passivation scheme comprises at least a wire-bonding pad and said wire-bonding pad is connected to a conductive wire by a wirebonding process.~~

24. (currently amended) The electronic component ~~chip structure~~ of Claim 23, wherein said patterned circuit layer comprises a metal trace connecting said second and third portions. ~~wire-bonding pad is electrically connected to said testing pad and/or said bump pad.~~

25. (currently amended) The electronic component ~~chip structure~~ of Claim 1, wherein the pitch ~~distance~~ between said first and second portions ~~bump pad and said testing pad~~ is less ~~smaller~~ than 300 μm.

26. (currently amended) The electronic component ~~chip structure~~ of Claim 1, wherein the pitch ~~distance~~ between said first and second portions ~~bump pad and said testing pad~~ is less ~~smaller~~ than 1 millimeter.

27. (currently amended) An electronic component ~~chip structure,~~ comprising:

a semiconductor substrate; ~~having a plurality of electronic devices positioned on or in a surface layer of said semiconductor substrate;~~

a metallization structure over said semiconductor substrate; ~~fine line interconnection scheme comprising:~~

~~a plurality of dielectric layers over said semiconductor substrate and said dielectric layers having a plurality of via holes; and~~

~~a plurality of circuit layers each on one of said dielectric layers, wherein said circuit layers are electrically connected to each other through said via holes and are electrically connected to said electronic devices;~~

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and~~said fine line interconnection scheme, wherein said passivation layer comprises at least a opening exposing one of said circuit layer;~~

a patterned circuit layer connected to said top surface, wherein said patterned circuit layer comprises a first portion having a bump formed thereover and a second portion used to be wirebonded thereto. ~~a post-passivation scheme over said passivation layer, wherein said post-passivation scheme comprises at least a metal layer electrically connected to said circuit layers, wherein said metal layer comprises a gold layer having a thickness larger than 1 μm and said metal layer comprises at least a bump pad and at least a wire-bonding pad;~~

~~at least a bump disposed on said bump pad; and~~

~~at least a conductive wire connected to said wire-bonding pad by a wirebonding process.~~

28. (currently amended) The electronic component ~~chip structure~~ of Claim 27, wherein said patterned circuit layer comprises gold. ~~metal layer further comprises an adhesion/barrier layer underlying said gold layer.~~

29. (currently amended) The electronic component ~~chip structure~~ of Claim 27 ~~28~~, wherein said patterned circuit layer comprises copper. ~~said material constituting said adhesion/barrier layer is selected from a group consisting of chromium, titanium, tantalum, titanium-tungsten alloy, tantalum nitride and titanium nitride.~~

30. (currently amended) The electronic component ~~chip structure~~ of Claim 27 further comprising a polymer layer over said passivation layer, wherein said patterned circuit layer is over said polymer layer. ~~post-passivation scheme further comprises a polymer layer disposed between said metal layer and said passivation layer.~~

31. (currently amended) The electronic component ~~chip structure~~ of Claim 30, wherein said polymer layer comprises ~~is made of~~ polyimide, ~~, benzocyclobutene, porous dielectric material, parylene, epoxy, solder mask material or elastomer.~~

32. (currently amended) The electronic component ~~chip structure~~ of Claim 27 comprising a polymer layer on said patterned circuit layer, an opening in said polymer layer exposing said first portion. ~~, wherein said post passivation scheme further comprises a polymer layer covering said metal layer.~~

33. (currently amended) The electronic component ~~chip structure~~ of Claim 32, wherein said polymer layer comprises ~~is made of~~ polyimide, ~~, benzocyclobutene, porous dielectric material, parylene, epoxy, solder mask material or elastomer.~~

34. (currently amended) The electronic component ~~chip structure~~ of Claim 27, wherein said patterned circuit layer comprises a metal trace connecting said first and second portions. ~~post passivation scheme further comprises a plurality of metal layers.~~

35. (currently amended) The electronic component ~~chip structure~~ of Claim 27, wherein said patterned circuit layer comprises a third portion used to be tested thereto. ~~metal layer comprises at least a testing pad and at least a metal line and said metal line connects said bump pad to said testing pad.~~

Claim 36 (canceled)

37. (currently amended) The electronic component ~~chip structure~~ of Claim 35 ~~27~~, wherein the pitch between said first and second portions is less than 300 μm. ~~said opening of said passivation layer has a width larger than about 0.1 um.~~

38. (currently amended) The electronic component ~~chip structure~~ of Claim 27, wherein said passivation layer has a thickness greater ~~larger~~ than 0.35 μm.

39. (currently amended) The electronic component ~~chip structure~~ of Claim 27, wherein said passivation layer comprises a topmost nitride layer of said electronic component. ~~is a silicon oxide layer, a silicon nitride layer, a phosphosilicate glass (PSG) layer, a silicon oxide nitride layer or a composite structure comprising said above mentioned layers.~~

40. (currently amended) The electronic component ~~chip structure~~ of Claim 27 further comprising a bump over said first portion. ~~, wherein said metal layer has a thickness larger than 0.4 μm.~~

41. (currently amended) The electronic component ~~chip structure~~ of Claim 40 ~~27~~, wherein said bump comprises solder. ~~a solder metal and an under bump metallurgy layer, said under-~~

~~bump metallurgy layer is disposed on said bump pad and said solder metal is disposed on said under bump metallurgy layer.~~

42. (currently amended) The electronic component ~~chip structure~~ of Claim 40~~-41~~, further comprising a copper layer between said bump and said first portion. ~~wherein said under bump metallurgy layer is formed, from the bottom to the top, from a titanium layer, a copper layer and a nickel layer.~~

43. (currently amended) The electronic component ~~chip structure~~ of Claim 40~~-41~~, wherein said bump comprises a lead-free alloy. ~~a material constituting said solder metal is selected from a group consisting of a tin lead alloy and a lead free solder alloy.~~

44. (currently amended) The electronic component ~~chip structure~~ of Claim 27 further comprising a wirebonded wire bonded over said second portion. ~~, wherein said metal layer further comprises at least a testing pad electrically connected to said bump pad and the distance between said bump pad and said testing pad is smaller than 300 μm.~~

Claim 45 (canceled)

46. (newly added) An electronic component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and

a patterned circuit layer connected to said top surface, wherein said patterned circuit layer comprises a first portion used to be wirebonded thereto and a second portion used to be tested thereto.

47. (newly added) The electronic component of Claim 46, wherein said patterned circuit layer comprises gold.

48. (newly added) The electronic component of Claim 46, wherein said patterned circuit layer comprises a gold layer having a thickness greater than 1 micron.

49. (newly added) The electronic component of Claim 46, wherein said patterned circuit layer comprises copper.

50. (newly added) The electronic component of Claim 46, wherein said patterned circuit layer comprises nickel.